## REMARKS

Claims 1-10 and 26-33 remain in the application. Claims 11-25 have been cancelled.

By this amendment, applicants have amended claims 1 and 26 to more particularly point out and distinctly claim the subject matter that applicants regard as their invention. Applicants' specification at paragraph [0027] and FIGS. 2-6 support the changes to claims 1 and 26

## Response to First 35 U.S.C. §103(a) Rejection

Claims 1-10 and 26-33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davies (USP 6,512,283) in view of Kadosh et al. (USP 6,069,398). This rejection is respectfully traversed in view the amendments made herein and the remarks made hereinafter.

Claim 1 has been amended to call for semiconductor substrate having a surface formed with a first recessed region that is substantially filled with a first dielectric material. A second recessed region is formed within the first dielectric material, and the second recessed region has walls, a lower surface, and an opening in proximity to the surface. Additionally, a semiconductor layer is formed overlying the first dielectric material and adjoining the opening. A thermal oxide layer is formed intermixed with the semiconductor layer, wherein the thermal oxide layer seals the opening in the second recessed region while leaving a void in the second recessed region.

In Davies, first recessed regions 200 are formed in substrate 10, but regions 200 are not substantially filled

with a first dielectric. Regions 200 are merely lined with a thin dielectric layer 15'. Also, Davies does not have a second recessed region formed within the first dielectric material 15'. In Davies' FIG. 9, his second recessed regions 21 are actually formed in the semiconductor substrate 10. Further, Davies' does not suggest that regions 21 are formed in a dielectric material that substantially fills the first recessed regions 200.

Additionally, Davies does not show or suggest a semiconductor layer formed overlying first dielectric material 15' and adjoining an opening in the second recessed region. Clearly, layer 15 in Davies' FIG. 9 is a silicon dioxide layer (see Col. 6, lines 3-4), and the mere mention of a polysilicon resistor in Col. 4, lines 19-22 does not show or suggest the placement of it as expressly called for in claim 1. In fact, the teaching of Davies would suggest that the polysilicon resistor is no where near the opening, but instead is placed on top of oxide 56, which would clearly prevent the semiconductor layer from adjoining the opening as called for claim 1.

Turning now to the Kadosh reference for consideration, applicants first submit that there is no motivation to combine Davies and Kadosh because Kadosh has nothing to do with forming dielectrically isolated regions within a substrate. In particular, the Kadosh reference pertains to forming a thin film resistor that is elevated above the substrate (see Col 1, lines 7-11).

Even assuming *arguendo* that there is motivation to combine the two references, the Kadosh reference still does not make up for the deficiencies of the Davies reference set forth above. Moreover, the Kadosh reference does not show or suggest a thermal oxide layer intermixed with a

semiconductor layer. Instead, Kadosh's polysilicon regions 36 are separate and distinct from the oxide layer 26.

Thus, for at least the above reasons, applicants respectfully submit that Davies in view of Kadosh fails to make claim 1 obvious.

Claims 2-10 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 26 has been amended and now calls for a semiconductor device, comprising a semiconductor substrate having a surface formed with a first recessed region. A first dielectric material is deposited in the first recessed region and is further formed with a second recessed region having an opening and walls, and the first dielectric material substantially fills the first recessed region. A semiconductor cap layer is formed adjoining edges of the opening. A thermal oxide layer is merged with the semiconductor layer to seal the opening.

Applicants respectfully submit that the combination of Davies and Kadosh fails to make claim 26 obvious for at least the following reasons. First, applicants reiterate that there is no motivation to combine references as set forth above in their response to the rejection of claim 1.

However, assuming *arguendo* that there is such motivation, neither reference shows or suggests a first recessed region substantially filled with a first dielectric material. Davies' first recessed region 200 is merely lined with a thin dielectric layer 15', and Kadosh does not even show or suggest a first recessed region formed in a semiconductor substrate. Also, Davies does not show or suggest a second recessed region formed in the first dielectric material. In Davies, recessed regions 21 are actually formed in semiconductor substrate 10. Kadosh

does not show or suggest a second recessed region at all. Additionally, neither reference shows or suggests a semiconductor cap layer formed adjoining edges of the opening. In Davies, a silicon oxide layer 15 adjoins edges of the Davies opening. Moreover, the polysilicon resistor referred to in Col. 4 in Davies would be at best separated from the Davies' openings by an oxide layer 56, so it would be impossible for the resistor structures suggested by Davies to adjoin edges of the opening as is expressly called for in claim 26. Further, neither reference shows or suggests a thermal oxide layer merged with the semiconductor cap layer. In both references, the shown or suggested semiconductor layers are separate and distinct layers that are not merged with a thermal oxide as is called for in claim 26. Thus, for at least these reasons, applicants respectfully submit that claim 26 is allowable over Davies and Kadosh.

Claims 27-33 depend from claim 26 and are believed allowable for at least the same reasons as claim 26.

Response to Second 35 U.S.C. §103(a) Rejection

Claims 1-10 and 26-33 were rejected under 35 U.S.C. §103(a) as being obvious in view of Lur et al., USP 5,640,041. This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 has been amended to call for semiconductor substrate having a surface formed with a first recessed region that is substantially filled with a first dielectric material. A second recessed region is formed within the first dielectric material, and the second recessed region

has walls, a lower surface, and an opening in proximity to the surface. Additionally, a semiconductor layer is formed overlying the first dielectric material and adjoining the opening. A thermal oxide layer is formed intermixed with the semiconductor layer, wherein the thermal oxide layer seals the opening in the second recessed region while leaving a void in the second recessed region.

Applicants respectfully submit that Lur fails to make claim 1 obvious because Lur does not show or suggest a semiconductor layer formed overlying the first dielectric material, adjoining the opening and further intermixed with a thermal oxide layer to seal the opening of the second recessed region. In Lur, layer 5 is formed away from the opening of the recessed region, and layer 5 is not intermixed with oxide layer 25. Instead layer 5 is a separate and distinct layer. Thus, applicants respectfully submit that claim 1 is allowable for at least these reasons.

Claims 2-10 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 26 has been amended and now calls for a semiconductor device, comprising a semiconductor substrate having a surface formed with a first recessed region. A first dielectric material is deposited in the first recessed region and is further formed with a second recessed region having an opening and walls, and the first dielectric material substantially fills the first recessed region. A semiconductor cap layer is formed adjoining edges of the opening. A thermal oxide layer is merged with the semiconductor cap layer to seal the opening.

Applicants respectfully submit that Lur fails to make claim 26 obvious because Lur does not show or suggest a

semiconductor cap layer formed adjoining edges of the opening and further merged with a thermal oxide layer to seal the opening. In Lur, layer 5 is formed away from the opening of the recessed region, not adjoining the edges of the opening as is called for in claim 26. Additionally, layer 5 is not merged with oxide layer 25. Instead layer 5 is a separate and distinct layer. Thus, applicants respectfully submit that claim 26 is allowable for at least the same reasons.

Claims 27-33 depend from claim 26 and are believed allowable for at least the same reasons as claim 26.

Applicants have further reviewed the cited but not relied upon references in the present Office Action and respectfully submit that these references are not more relevant than the relied upon references.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

In view of the fact that this application has been pending since February 7, 2002, and separately prosecuted extensively under Examiners Thomas Magee and Eddie Lee, applicants' undersigned attorney respectfully requests that Examiner Nadav contact him by telephone to discuss any further issues with this case if any remain after this amendment.

Respectfully submitted,

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